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EFFECT OF DRIFT REGION DOPING AND COULMN THICKNESS VARIATIONS IN A SUPER JUNCTION POWER MOSFET: A 2-D SIMULATION STUDY

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In this paper, a power SJMOSFET (Super junction MOSFET) transistor is simulated using PISCES-II, a 2-D numerical device simulator. The doping densities and device dimensions are chosen so as to simulate a typical device structure. These simulations are aimed at understanding the device physics through various electrical quantities like potential distribution, electric field distribution, and electron concentrations etc. in different regions of the device both in on/off states. The effects of doping variations in the 'n' and 'p' pillars of the SJMOSFET along with the variations in the column thickness of the device were investigated. Various results obtained reveal that device having equal doping in the n and p pillars and having equal width of these pillars gives the best results. The current density is maximum and the charge imbalance is minimum for this case, however the breakdown voltage increases when the width of the n pillar is decreased.

Keywords: *SUPER JUNCTION (SJMOSFET), COOLMOS, POWER MOSFET, DEVICE SIMULATION.*

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1. INTRODUCTION

The major limiting factor in conventional power MOSFETs is the square law dependence of the on-state resistance (R_{on}) on the breakdown voltage (BV). The reason for a large R_{on} for a power MOSFET is that in order to reduce the electric field at the junction, the doping level of the epitaxial layer has to be reduced. As a consequence, the epitaxial thickness must be made larger which directly results in an increase in R_{on}. Since the R_{on} of power MOSFETs increases sharply with the breakdown voltage, this has prevented the use of power MOSFETs at high voltages. There exists a trade-off relationship between specific on-state resistance (R_{on}) and breakdown voltage (BV) for conventional power MOSFETs which limits the application of power MOSFETs in many fields. It can be shown that R_{on} is proportional to $BV^{2.5}$ for a VDMOS (vertical double-diffused MOSFET) transistor. This relation ($R_{on} \propto BV^{2.5}$) is referred to as the "Silicon Limit". In order to overcome the disadvantage of power MOSFETs, Superjunction (SJ) concept was proposed to overcome the theoretical (conventional) silicon limit. Recently, the invention of superjunction [1-8] (SJ) MOSFET has made it possible to attain higher speeds and larger breakdown voltages simultaneously. The structure of the superjunction (SJ) shown in Fig. 1 is fairly complex and different from the conventional MOS structure because of the existence of superjunction drift

layer. In these devices [1-6], a superjunction composed of p and n pillars, which share vertical boundaries, replaces the drift layer. This modification causes a noticeable change in the electric field profile with in the device, thereby resulting in large breakdown voltage. The superjunction devices are based on the principle of charge compensation, which has been derived from the lateral *RESURF* (Reduced Surface Field) idea. The doping level of n pillars can be greater than that of the conventional power MOSFETs and the

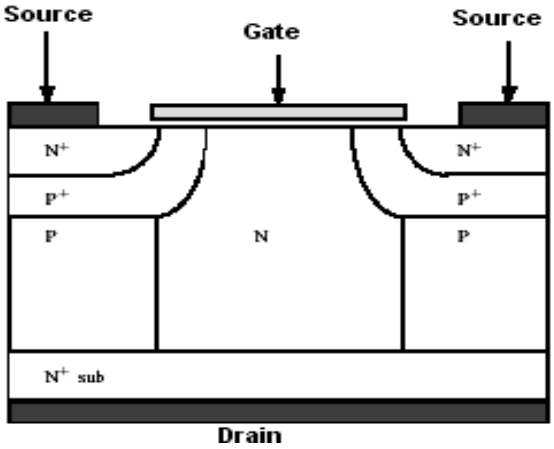

Fig. 1 *– Schematic design of Superjunction MOSFET. Structure shown represents one cell of the device*

excess charge in the n pillar can be counter balanced by the adjacent charges in the *p* pillar, thus contributing to a horizontal electrical field without affecting its vertical field distribution. Accordingly, *SJ MOSFET* concept can realize very low on-resistance by increasing the aspect ratio of n and p pillars because the negative and positive charges in each pillar can easily compensate each other to allow increase in their doping concentration [1]. However, in reality, the superjunction structure has the following difficulties: (1) The charge must be strictly controlled in the pillars; otherwise the breakdown voltage decrease rapidly; (2) Deep doping into bulk to make pillars is required to minimize the number of iteration processes; (3) As the total imbalanced charge increases with pillar depth, the realization of high voltage devices becomes increasingly difficult; (4) In addition, it is very difficult to make deep implantation due to crystalline damage caused by high-energy implants.

Recently a 600 V superjunction power MOSFET (CoolMOS^{TM}) has been introduced commercially by the Infineon Technologies [7] SPP20N60S5 having R_{on} equal to 0.19 Ohm·cm^2. CoolMOS^{TM} is a new revolutionary technology for high voltage power MOSFETs and it implements a compensation structure in the vertical drift region of a MOSFET in order to improve the on-state resistance. Such a structure makes it possible to reduce the on-state resistance (R_{on}) of a 600V MOSFET by a factor of 5 for the same chip area. It is claimed that the CoolMOS^{TM} achieves the fastest switching given the same chip size. Compared to a traditional VDMOSFET with the same chip area, CoolMOS^{TM} offers extremely low static and dynamic losses.

In this paper, we have studied the effect of doping and thickness variations of the n and p pillars with the help of a 2-D device simulator PISCES-II. The device dimensions are chosen so as to simulate a typical device structure. These simulations are aimed at understanding the device physics through various electrical quantities like potential distribution, electric field distribution, and electron concentrations etc. in different regions of the device both in on/off states. The I-V characteristics were compared for different devices for various gate and drain voltages. The effects of doping variations in the 'n' and 'p' pillars of the SJMOSFET along with the variations in the column thickness of the device were investigated. Various results obtained reveal that that device having equal doping in the n and p pillars and having equal width of these pillars gives the best results. The current density is maximum and the charge imbalance is minimum for this case; however the breakdown voltage increases when the width of the n pillar is decreased.

2. SJ -MOSFET STRUCTURE AND OPERATION

Fig. 2 shows a cross section of a SJ-MOSFET. The various design parameters used for simulation are shown in the table 1. This structure allows a doping level of the n-region, which is typically one order of magnitude higher than that in standard high-voltage MOSFETs. The additional charge is counterbalanced by the adjacent charges of the p-column, thus contributing to a horizontal electrical field without affecting the vertical field distribution. Along with the efforts of exploring circuit topologies, the device technology is also continuously improved. New devices such as CoolMOS^{TM} have come into commercial production recently as mentioned above, although the cost is high. The physics of operation of Superjunction power MOSFET as shown in Fig. 2 is different from that for the conventional power MOSFET structures.

Without the application of a gate bias i.e., when the device is in the off state, a high voltage can be supported in the Superjunction MOSFET structure when a positive bias is applied to the drain. In this case, vertical junction J2 formed between the p-type drift region and the n-type drift region becomes reverse biased. Simultaneously the drain voltage is applied across the horizontal MOS structure formed between the gate electrode on the upper surface of the n-type drift region as well as the horizontal junction J3 formed between the p-type drift region and the n buffer layer. The MOS structure operates in the deep depletion mode due to the presence of the reverse bias across junction J2 between the p-type drift region and the n-type drift region. Consequently, depletion regions are formed across the vertical junction J2 and the horizontal MOS interface creating the desired two-dimensional charge coupling phenomenon. Simultaneously depletion regions are formed across the vertical junction J2 and the horizontal junction J3 creating a two-dimensional depletion phenomenon. These two dimensional depletion phenomenon alter the electric field distribution along the y-direction from the triangular shape observed in the conventional parallel-plane junctions to a rectangular shape. This allows supporting a required blocking voltage over a shorter distance. In addition, the doping concentration in the n-type drift region can be made much greater than that predicted by the one-dimensional theory. This allows substantial reduction of the specific on-state resistance to below the ideal

specific on-state resistance at any desired breakdown voltage. Drain current flow in the Superjunction power MOSFET structure is induced by the application of a positive bias to the gate electrode ($V_{gs} > V_t$). This produces an inversion layer at

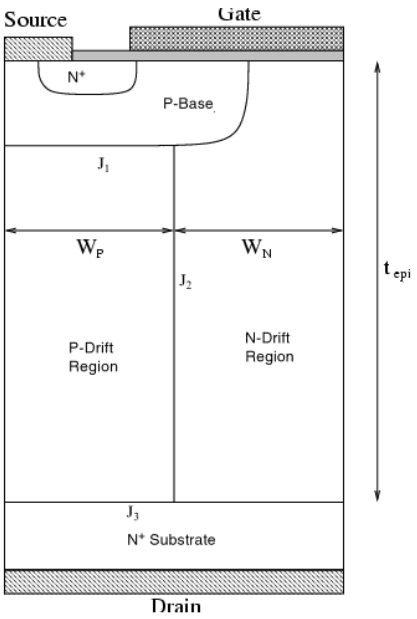

Fig. 2 *– Cross section of a SJ MOSFET*

Table 1 *– Design parameters used for SJMOSFET Simulation*

Parameter	Value
W_P, μm	2.0
W_N, μm	2.0
t_{ox}, μm	0.08
t_{epi}, μm	16
N_{n-}, $\times 10^{15}$ cm^{-3}	5.0
N_{n+}, $\times 10^{19}$ cm^{-3}	1.0
N_p, $\times 10^{17}$ cm^{-3}	2.0

the surface of the p-base region at the upper surface. The inversion layer channel provides a path for transport of electrons from the source to the n-type drift region when a positive drain voltage is applied. After transport from the source region through the channel, the electrons enter the n-type drift region and are then transported vertically down to the N_+ substrate. The resistance of the drift region is very low in the superjunction power MOSFET structure due to the high doping concentration in the n-type drift region (an accumulation layer forms at the upper surface under the gate electrode which reduces the on resistance by distributing the current into the n-type drift

region). The channel resistance in the Superjunction power MOSFET structure is small due to the small cell pitch or high channel density.

3. SIMULATION RESULTS AND DISCUSSIONS

Table 2 below shows the various doping variations used in various devices simulated so as to understand the effect of having different doping densities in the n and p pillars of the device. We have studied four different combinations of the doping densities and studied the effect of these variations with the help of various simulation results. Fig. 3 shows that with the increase in the 'p' pillar doping potential within the device along the vertical axis in the drift region gradually decrease when the device is in the on-state.

Table 2 – *Doping variations in various simulated devices*

Device Name	N-pillar Doping,$\times 10^{15}$ cm^{-3}	P-pillar Doping,$\times 10^{15}$ cm^{-3}
Device 1	5.0	5.0
Device 2	5.0	6.0
Device 3	5.0	7.0
Device 4	5.0	9.0

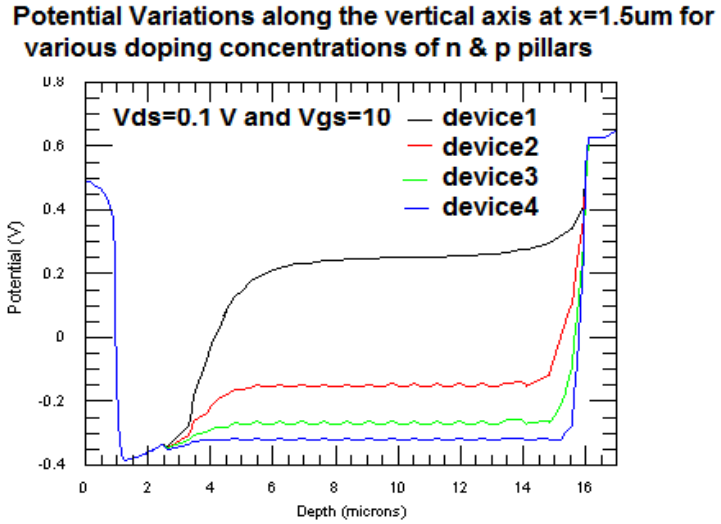

Fig. 3 – *Potential variations in the on-state for various device*

When both n and p pillars are at the same doping levels the drift region of the device is almost at the zero potential at the edge of the boundary of the p-pillar. This means that the negative and positive charges balance each other when these two regions are at the same doping levels.

Fig. 4 shows that the electric field within these devices in the on state is well with in the critical field of the silicon devices. The figure further tells us that there is not much variation in the electric field with the change in the p-pillar doping concentration. Fig. 5 gives the comparison of electron concentration variations in the on-state with the change in the drift region

doping of the p-pillar. The electron concentrations within the drift region of the device tend to decrease so as to create charge imbalance during the on

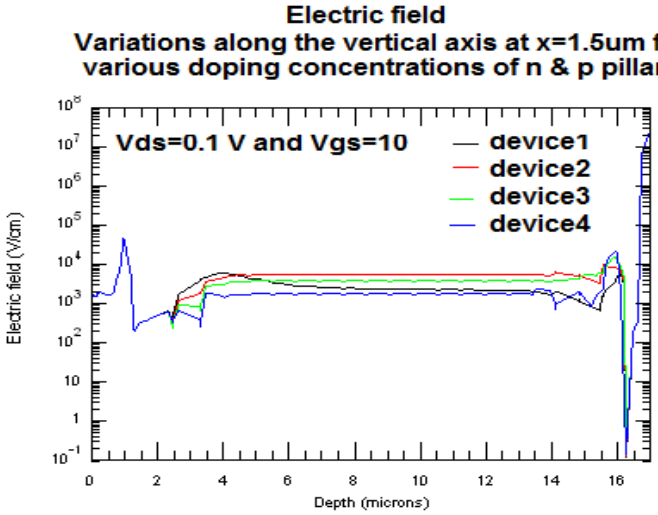

Fig. 4 *– Electric field variations in the on-state for various devices*

state. Thus we can conclude that device having equal doping in the n and p pillars (Device 1) gives the best results. The potential distribution and electron concentrations tend to decrease with the increase in the doping of the p-pillar whereas the electric field distribution almost remains uniform along the vertical axis within the middle of the drift region. Therefore, we can say that the charge imbalance is minimum for this case (Device 1).

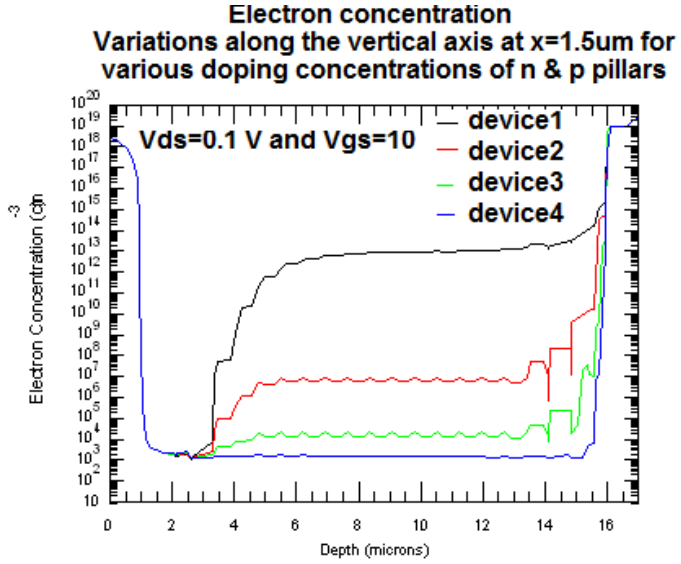

Fig. 5 *– Electron concentration variations in the on-state*

Table 3 gives the various combinations used in simulating different SJ-MOSFETs with varying widths of n and p pillars. Various simulation results obtained from these devices have been obtained to study the effect of variation of the width of n and p pillars.

Table 3 – *Width variations in various simulated devices*

Device Name	Width of N-pillar	Width of P-pillar
CM 1	2.0μm	2.0μm
CM 2	3.0μm	1.0μm
CM 3	1.0μm	3.0μm
CM 4	1.5μm	2.5μm
CM 5	0.8μm	3.2μm

Fig. 6 gives the comparison of the net charge within these devices and suggests that the device CM1 where both the n and p pillars having the same width have the minimum imbalance.

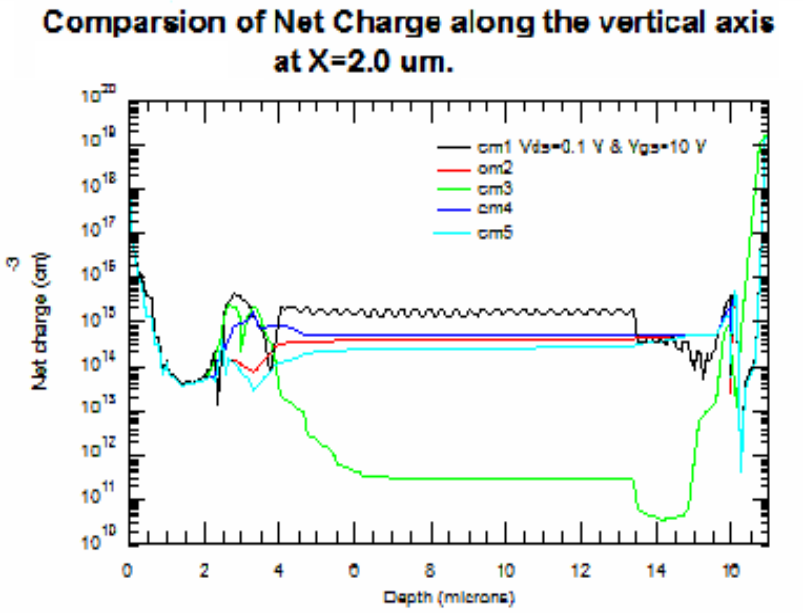

Fig. 6 – *Comparison of net charge in the on-state w.r.t. the variation in the pillar width*

In Fig. 7a–d the various I-V characteristics obtained from these simulations suggests that the current density is maximum for the device with equal width of n and p pillars (device CM1) in the on state for different values of V_{ds} and V_{gs}; however in the off state ie when $V_{gs} = 0$ V, the device having the least width for the n pillar supports a larger forward blocking voltage i.e., the breakdown voltage.

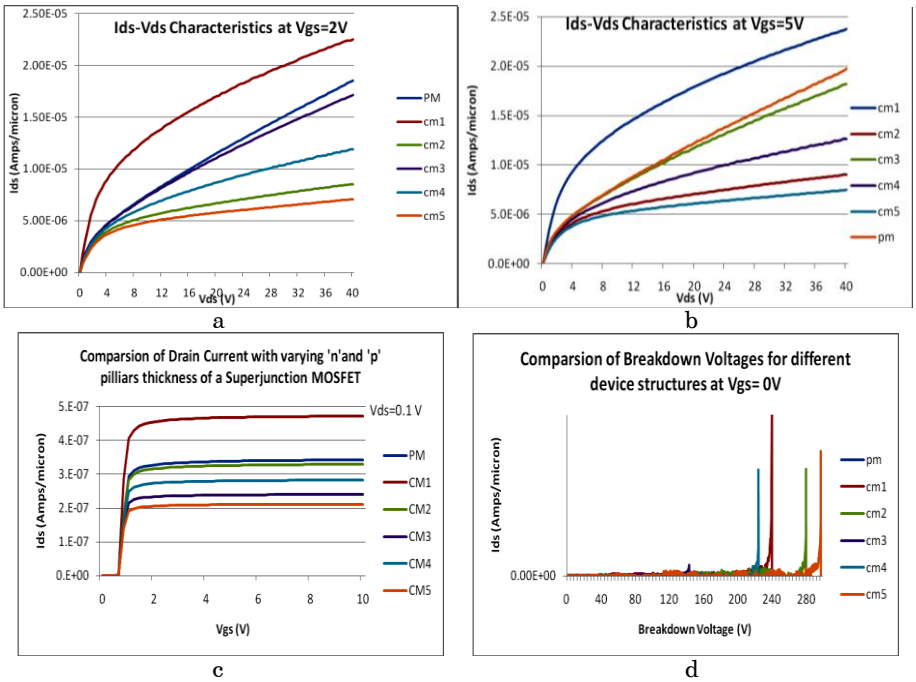

Fig. 7 – *Various I-V characteristics for the simulated devices at* $V_{gs} = 2$ *V* (a), $V_{gs} = 5$ *V* (b), $V_{gs} = 0.1$ *V* (c) *and* $V_{gs} = 0$ *V* (d)

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